



Low Cost, Single-Supply Differential Amplifier

AD626

FEATURES

Pin Selectable Gains of 10 and 100

True Single-Supply Operation

Single-Supply Range of +2.4 V to +10 V

Dual-Supply Range of ± 1.2 V to ± 6 V

Wide Output Voltage Range of 30 mV to 4.7 V

Optional Low-Pass Filtering

Excellent DC Performance

Low Input Offset Voltage: 500 μ V Max

Large Common-Mode Range: 0 V to +54 V

Low Power: 1.2 mW ($V_S = +5$ V)

Good CMR of 90 dB Typ

AC Performance

Fast Settling Time: 24 μ s (0.01%)

Includes Input Protection

Series Resistive Inputs ($R_{IN} = 200$ k Ω)

RFI Filters Included

Allows 50 V Continuous Overload

APPLICATIONS

Current Sensing

Interface for Pressure Transducers, Position Indicators,

Strain Gages, and Other Low Level Signal Sources

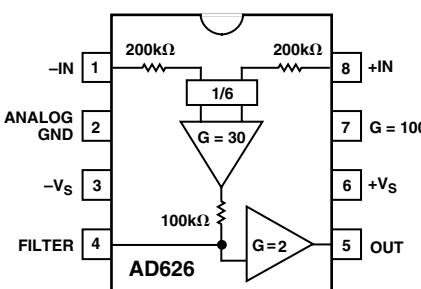
PRODUCT DESCRIPTION

The AD626 is a low cost, true single-supply differential amplifier designed for amplifying and low-pass filtering small differential voltages from sources having a large common-mode voltage.

The AD626 can operate from either a single supply of +2.4 V to +10 V, or dual supplies of ± 1.2 V to ± 6 V. The input common-mode

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N) and SOIC (R) Packages



range of this amplifier is equal to 6 ($+V_S - 1$ V) which provides a +24 V CMR while operating from a +5 V supply. Furthermore, the AD626 features a CMR of 90 dB typ.

The amplifier's inputs are protected against continuous overload of up to 50 V, and RFI filters are included in the attenuator network. The output range is +0.03 V to +4.9 V using a +5 V supply. The amplifier provides a preset gain of 10, but gains between 10 and 100 can be easily configured with an external resistor. Furthermore, a gain of 100 is available by connecting the G = 100 pin to analog ground. The AD626 also offers low-pass filter capability by connecting a capacitor between the filter pin and analog ground.

The AD626A and AD626B operate over the industrial temperature range of -40°C to $+85^\circ\text{C}$. The AD626 is available in two 8-lead packages: a plastic mini-DIP and SOIC.

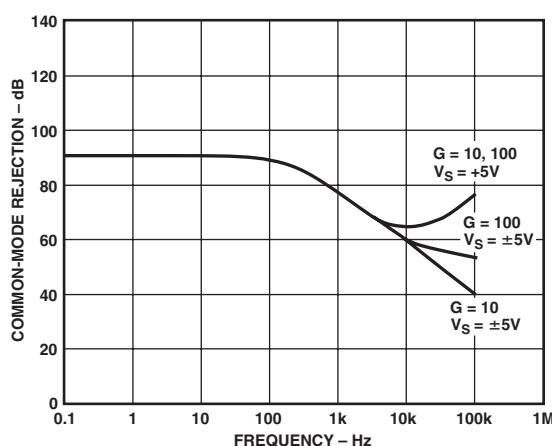


Figure 1. Common-Mode Rejection vs. Frequency

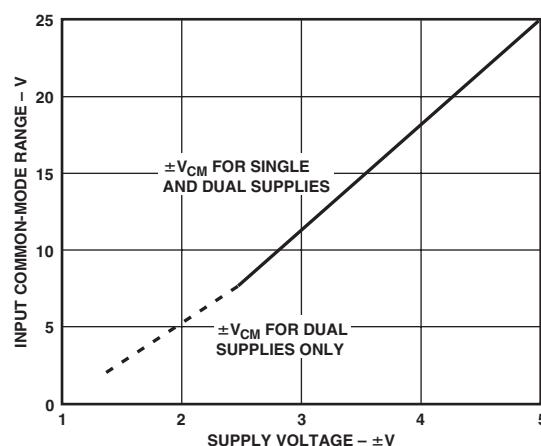


Figure 2. Input Common-Mode Range vs. Supply

REV. D

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AD626—SPECIFICATIONS

SINGLE SUPPLY (@ $+V_S = +5$ V and $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Model Parameter	Condition	AD626A			AD626B			Unit
		Min	Typ	Max	Min	Typ	Max	
GAIN								
Gain Accuracy	Total Error							
Gain = 10	@ $V_{\text{OUT}} \geq 100$ mV dc	0.4	1.0		0.2	0.6		%
Gain = 100	@ $V_{\text{OUT}} \geq 100$ mV dc	0.1	1.0		0.5	0.6		%
Over Temperature, $T_A = T_{\text{MIN}}$ to T_{MAX}	G = 10		50		30		120	ppm/ $^\circ\text{C}$
	G = 100		150					ppm/ $^\circ\text{C}$
Gain Linearity								
Gain = 10	@ $V_{\text{OUT}} \geq 100$ mV dc	0.014	0.016		0.014	0.016		%
Gain = 100	@ $V_{\text{OUT}} \geq 100$ mV dc	0.014	0.02		0.014	0.02		%
OFFSET VOLTAGE								
Input Offset Voltage		1.9	2.5		1.9	2.5		mV
vs. Temperature	T_{MIN} to T_{MAX} , G = 10 or 100	2.9			2.9			mV
vs. Temperature	T_{MIN} to T_{MAX} , G = 10 or 100	6			6			$\mu\text{V}/^\circ\text{C}$
vs. Supply Voltage (PSR)								
+PSR		74	80		74	80		dB
-PSR		64	66		64	66		dB
COMMON-MODE REJECTION								
+CMR Gain = 10, 100	$R_L = 10$ k Ω	66	90		80	90		dB
\pm CMR Gain = 10, 100	$f = 100$ Hz, $V_{\text{CM}} = +24$ V	55	64		55	64		dB
-CMR Gain = 10, 100*	$f = 10$ kHz, $V_{\text{CM}} = +6$ V	60	85		73	85		dB
	$f = 100$ Hz, $V_{\text{CM}} = -2$ V							
COMMON-MODE VOLTAGE RANGE								
+CMV Gain = 10	CMR > 85 dB		+24			+24		V
-CMV Gain = 10	CMR > 85 dB		-2			-2		V
INPUT								
Input Resistance								
Differential		200			200			k Ω
Common-Mode		100			100			k Ω
Input Voltage Range (Common-Mode)		6 ($V_S - l$)			6 ($V_S - l$)			V
OUTPUT								
Output Voltage Swing								
Positive	$R_L = 10$ k Ω	4.7	4.90		4.7	4.90		V
Gain = 10		4.7	4.90		4.7	4.90		V
Gain = 100		0.03			0.03			V
Negative		0.03			0.03			V
Short Circuit Current		12			12			mA
+ I_{SC}								
NOISE								
Voltage Noise RTI								
Gain = 10	$f = 0.1$ Hz–10 Hz	2			2			μV p-p
Gain = 100	$f = 0.1$ Hz–10 Hz	2			2			μV p-p
Gain = 10	$f = 1$ kHz	0.25			0.25			$\mu\text{V}/\sqrt{\text{Hz}}$
Gain = 100	$f = 1$ kHz	0.25			0.25			$\mu\text{V}/\sqrt{\text{Hz}}$
DYNAMIC RESPONSE								
-3 dB Bandwidth	$V_{\text{OUT}} = +1$ V dc	100			100			kHz
Slew Rate, T_{MIN} to T_{MAX}	Gain = 10	0.17	0.22		0.17	0.22		V/ μs
	Gain = 100	0.1	0.17		0.1	0.17		V/ μs
Settling Time	to 0.01%, 1 V Step	24			22			μs
POWER SUPPLY								
Operating Range	$T_A = T_{\text{MIN}}$ to T_{MAX}	2.4	5	12	2.4	5	10	V
Quiescent Current	Gain = 10		0.16	0.20		0.16	0.20	mA
	Gain = 100		0.23	0.29		0.23	0.29	mA
TRANSISTOR COUNT	Number of Transistors	46			46			

*At temperatures above 25°C, -CMV degrades at the rate of 12 mV/ $^\circ\text{C}$; i.e., @ 25°C CMV = -2 V, @ 85°C CMV = -1.28 V.

Specifications subject to change without notice.

DUAL SUPPLY (@ $+V_S = \pm 5$ V and $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Model Parameter	Condition	AD626A			AD626B			
		Min	Typ	Max	Min	Typ	Max	Unit
GAIN								
Gain Accuracy	Total Error							
Gain = 10	$R_L = 10 \text{ k}\Omega$	0.2	0.5		0.1	0.3		%
Gain = 100		0.25	1.0		0.15	0.6		%
Over Temperature, $T_A = T_{\text{MIN}}$ to T_{MAX}	$G = 10$			50			30	$\text{ppm}/^\circ\text{C}$
	$G = 100$			100			80	$\text{ppm}/^\circ\text{C}$
Gain Linearity								
Gain = 10		0.045	0.055		0.045	0.055		%
Gain = 100		0.01	0.015		0.01	0.015		%
OFFSET VOLTAGE								
Input Offset Voltage								
vs. Temperature	T_{MIN} to T_{MAX} , $G = 10$ or 100	50	500		50	250		μV
vs. Temperature	T_{MIN} to T_{MAX} , $G = 10$ or 100	1.0			0.5		0.5	mV
vs. Supply Voltage (PSR)								$\mu\text{V}/^\circ\text{C}$
+PSR		74	80		74	80		dB
-PSR		64	66		64	66		dB
COMMON-MODE REJECTION	$R_L = 10 \text{ k}\Omega$							
+CMR Gain = 10, 100	$f = 100 \text{ Hz}, V_{CM} = +24 \text{ V}$	66	90		80	90		dB
±CMR Gain = 10, 100	$f = 10 \text{ kHz}, V_{CM} = 6 \text{ V}$	55	60		55	60		dB
COMMON-MODE VOLTAGE RANGE								
+CMV Gain = 10	$\text{CMR} > 85 \text{ dB}$		26.5			26.5		V
-CMV Gain = 10	$\text{CMR} > 85 \text{ dB}$		32.5			32.5		V
INPUT								
Input Resistance								
Differential		200			200			$\text{k}\Omega$
Common-Mode		110			110			$\text{k}\Omega$
Input Voltage Range (Common-Mode)		6 ($V_S - l$)			6 ($V_S - l$)			V
OUTPUT								
Output Voltage Swing	$R_L = 10 \text{ k}\Omega$							
Positive	$\text{Gain} = 10, 100$	4.7	4.90		4.7	4.90		V
Negative	$\text{Gain} = 10$	-1.65	-2.1		-1.65	-2.1		V
	$\text{Gain} = 100$	-1.45	-1.8		-1.45	-1.8		V
Short Circuit Current								
$+I_{SC}$		12			12			mA
$-I_{SC}$		0.5			0.5			mA
NOISE								
Voltage Noise RTI								
Gain = 10	$f = 0.1 \text{ Hz}$ to 10 Hz	2			2			$\mu\text{V p-p}$
Gain = 100	$f = 0.1 \text{ Hz}$ to 10 Hz	2			2			$\mu\text{V p-p}$
Gain = 10	$f = 1 \text{ kHz}$	0.25			0.25			$\mu\text{V}/\sqrt{\text{Hz}}$
Gain = 100	$f = 1 \text{ kHz}$	0.25			0.25			$\mu\text{V}/\sqrt{\text{Hz}}$
DYNAMIC RESPONSE								
-3 dB Bandwidth	$V_{OUT} = +1 \text{ V dc}$		100			100		kHz
Slew Rate, T_{MIN} to T_{MAX}	$\text{Gain} = 10$	0.17	0.22		0.17	0.22		$\text{V}/\mu\text{s}$
	$\text{Gain} = 100$	0.1	0.17		0.1	0.17		$\text{V}/\mu\text{s}$
Settling Time	to 0.01%, 1 V Step		24			22		μs
POWER SUPPLY								
Operating Range	$T_A = T_{\text{MIN}}$ to T_{MAX}	± 1.2	± 5	± 6	± 1.2	± 5	± 6	V
Quiescent Current	$\text{Gain} = 10$	1.5	2		1.5	2		mA
	$\text{Gain} = 100$	1.5	2		1.5	2		mA
TRANSISTOR COUNT	Number of Transistors		46			46		

Specifications subject to change without notice.

AD626

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	+36V
Internal Power Dissipation ²		
Peak Input Voltage	+60V
Maximum Reversed Supply Voltage Limit	-34V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (N, R)	-65°C to +125°C
Operating Temperature Range		
AD626A/AD626B	-40°C to +85°C
Lead Temperature Range (Soldering 60 sec)	+300°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

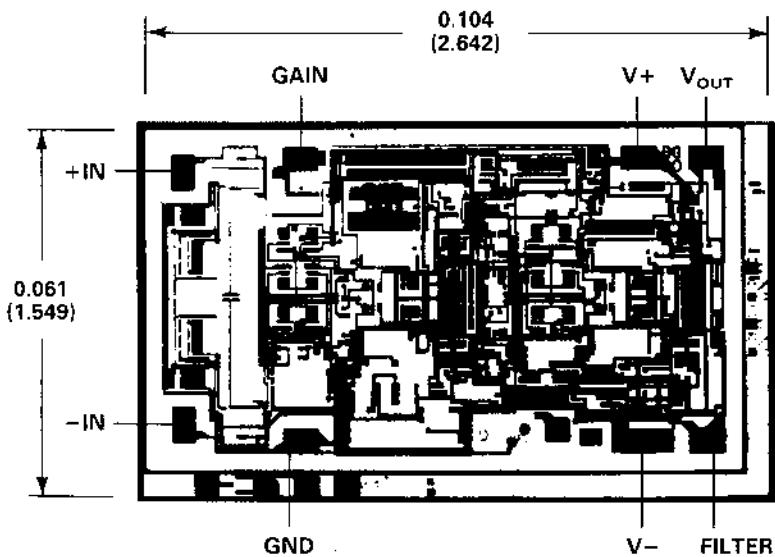
²8-Lead Plastic Package: $\theta_{JA} = 100^\circ\text{C}/\text{W}$; $\theta_{JC} = 50^\circ\text{C}/\text{W}$.
8-Lead SOIC Package: $\theta_{JA} = 155^\circ\text{C}/\text{W}$; $\theta_{JC} = 40^\circ\text{C}/\text{W}$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD626AN	-40°C to +85°C	Plastic DIP	N-8
AD626AR	-40°C to +85°C	Small Outline IC	R-8
AD626BN	-40°C to +85°C	Plastic DIP	N-8
AD626AR-REEL	-40°C to +85°C	13" Tape and Reel	
AD626AR-REEL7	-40°C to +85°C	7" Tape and Reel	

METALLIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).

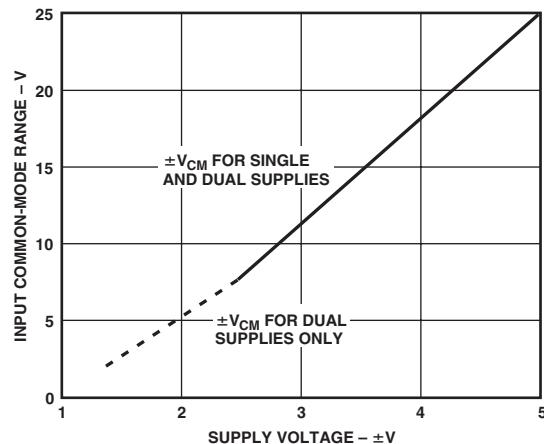


CAUTION

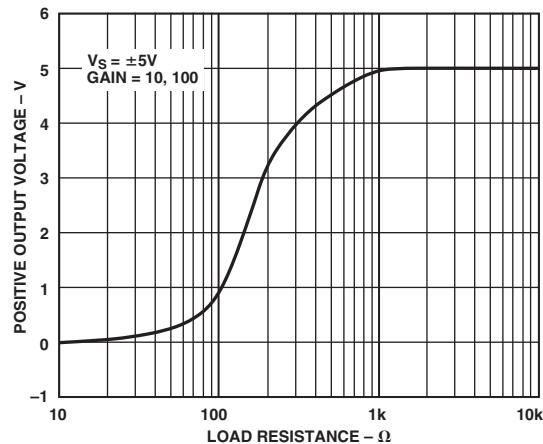
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD626 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



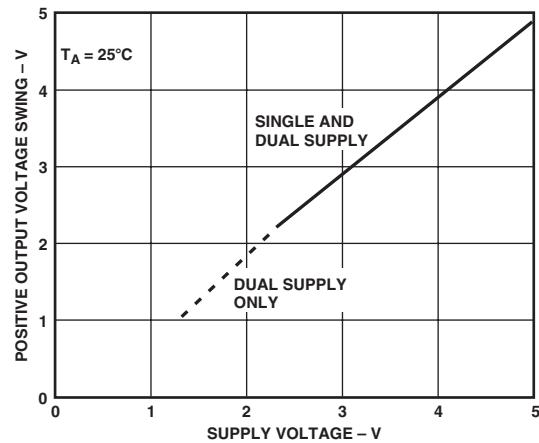
Typical Performance Characteristics—AD626



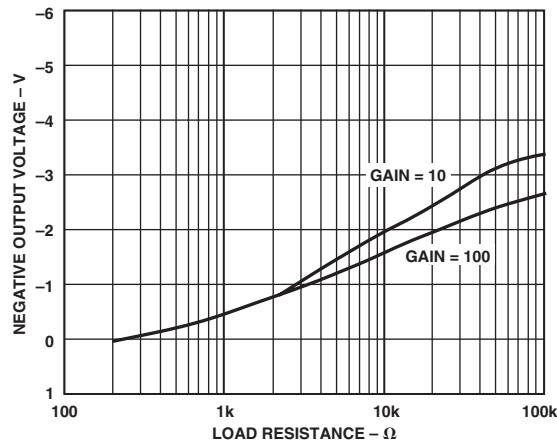
TPC 1. Input Common-Mode Range vs. Supply



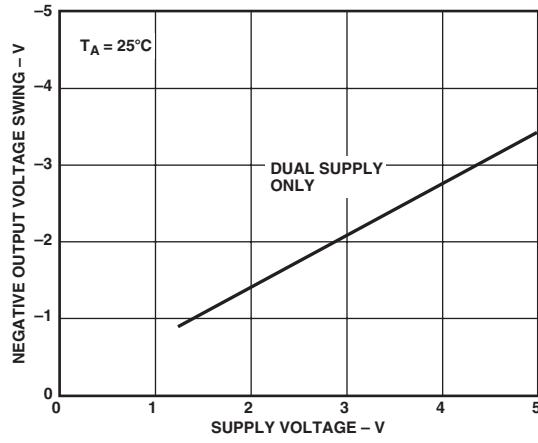
TPC 4. Positive Output Voltage Swing vs. Resistive Load



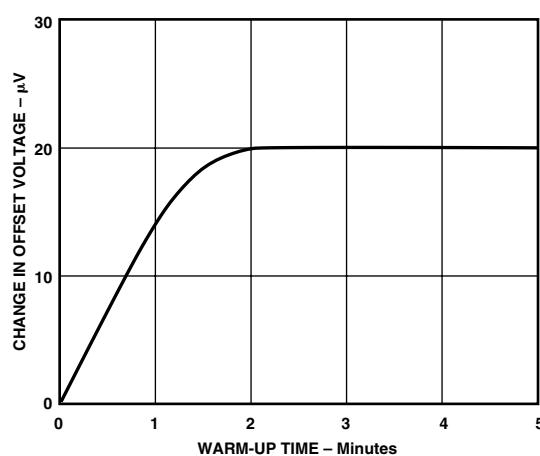
TPC 2. Positive Output Voltage Swing vs. Supply Voltage



TPC 5. Negative Output Voltage Swing vs. Resistive Load

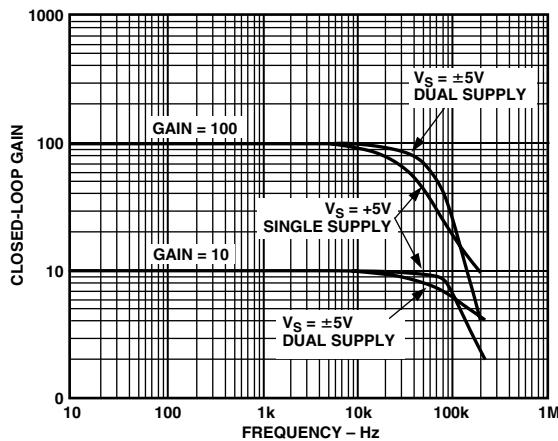


TPC 3. Negative Output Voltage Swing vs. Supply Voltage

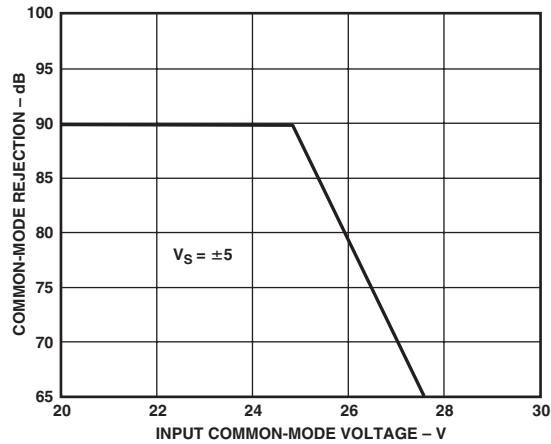


TPC 6. Change in Input Offset Voltage vs. Warm-Up Time

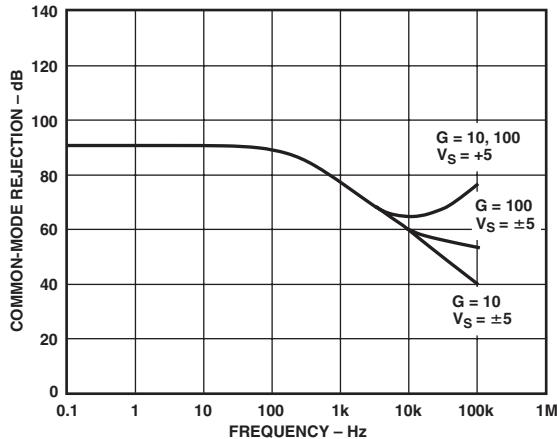
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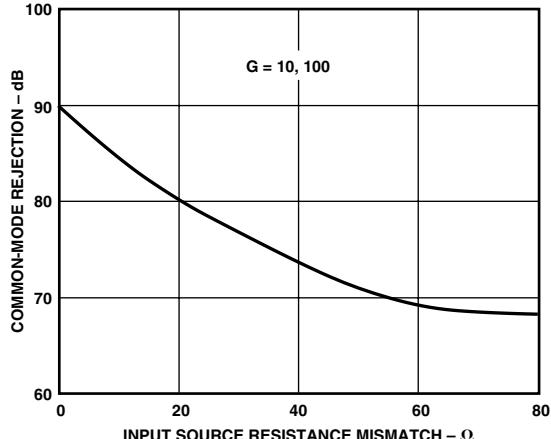
TPC 7. Closed-Loop Gain vs. Frequency



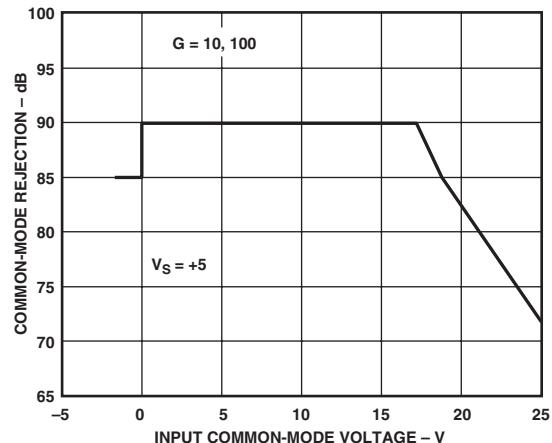
TPC 10. Common-Mode Rejection vs. Input Common-Mode Voltage for Dual-Supply Operation



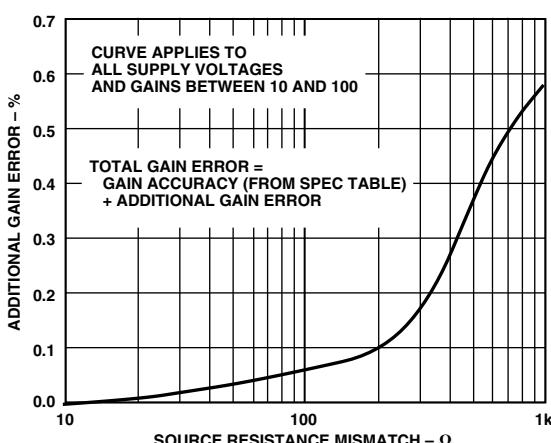
TPC 8. Common-Mode Rejection vs. Frequency



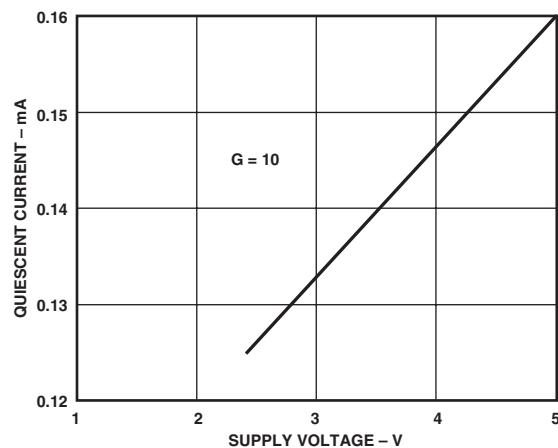
TPC 11. Common-Mode Rejection vs. Input Source Resistance Mismatch



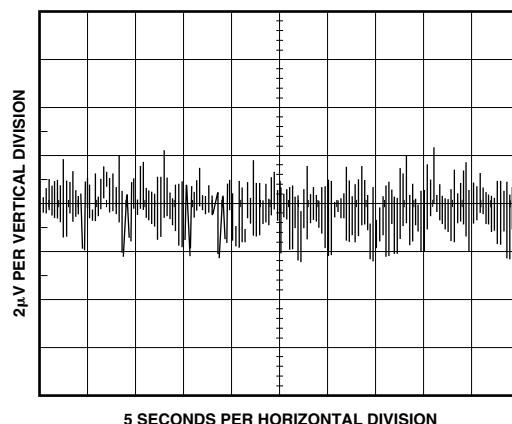
TPC 9. Common-Mode Rejection vs. Input Common-Mode Voltage for Single-Supply Operation



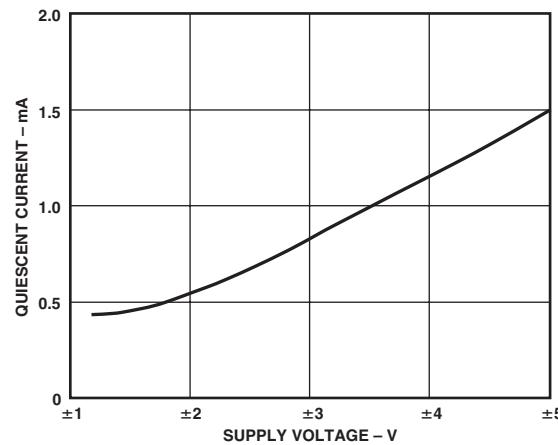
TPC 12. Additional Gain Error vs. Source Resistance Mismatch



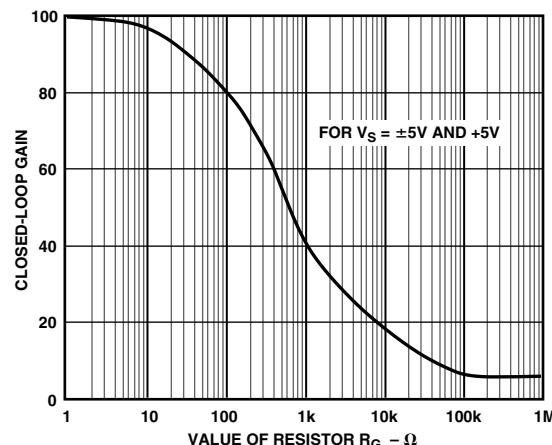
TPC 13. Quiescent Supply Current vs. Supply Voltage for Single-Supply Operation



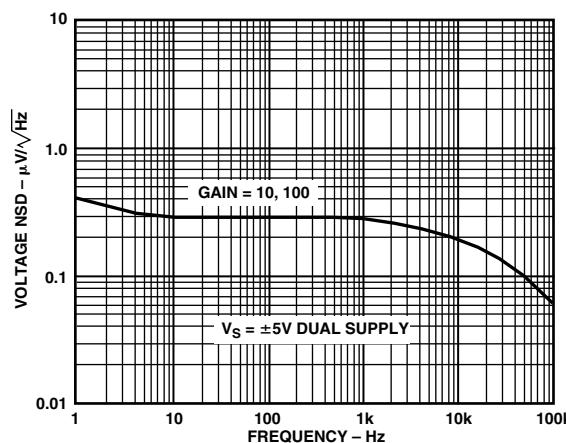
TPC 16. 0.1 Hz to 10 Hz RTI Voltage Noise. $V_S = \pm 5 V$, Gain = 100



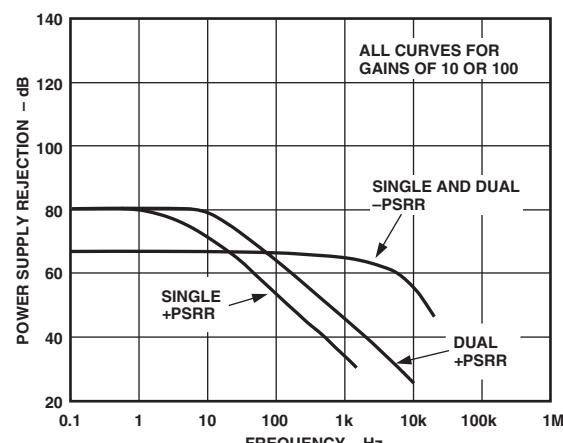
TPC 14. Quiescent Supply Current vs. Supply Voltage for Dual-Supply Operation



TPC 17. Closed-Loop Gain vs. R_G

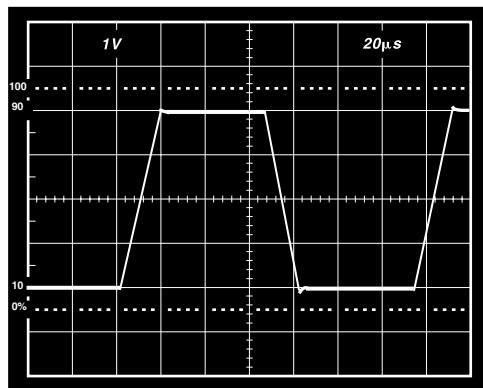


TPC 15. Noise Voltage Spectral Density vs. Frequency

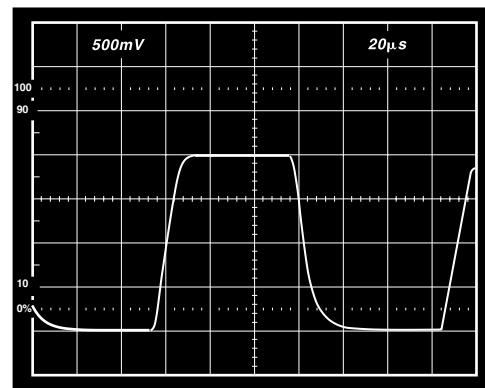


TPC 18. Power Supply Rejection vs. Frequency

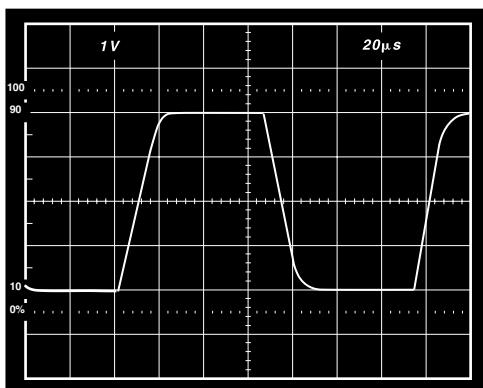
AD626



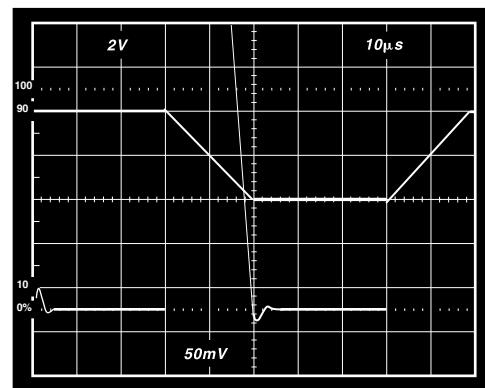
TPC 19. Large Signal Pulse Response. $V_S = \pm 5 V$, $G = 10$



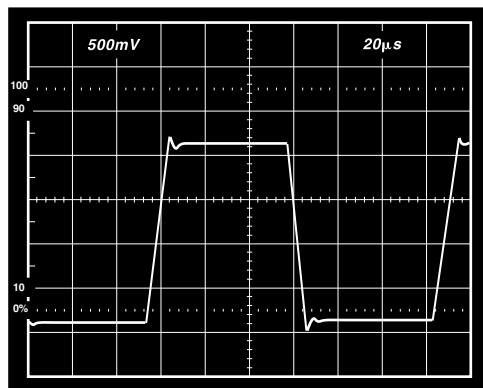
TPC 22. Large Signal Pulse Response. $V_S = +5 V$, $G = 100$



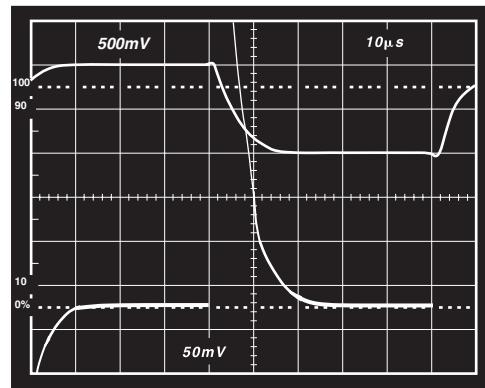
TPC 20. Large Signal Pulse Response. $V_S = \pm 5 V$, $G = 100$



TPC 23. Settling Time. $V_S = \pm 5 V$, $G = 10$



TPC 21. Large Signal Pulse Response. $V_S = +5 V$, $G = 10$



TPC 24. Settling Time. $V_S = \pm 5 V$, $G = 100$

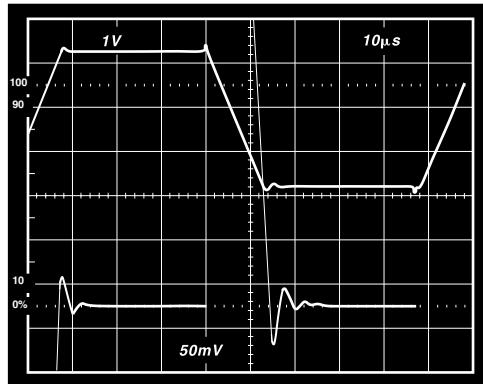
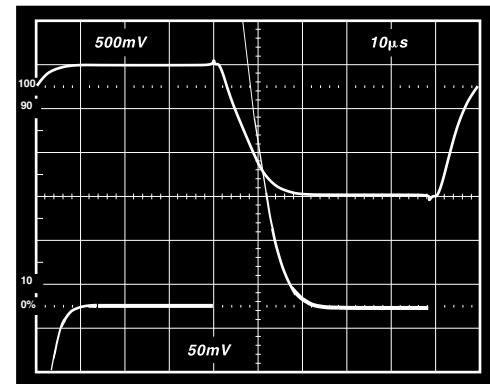
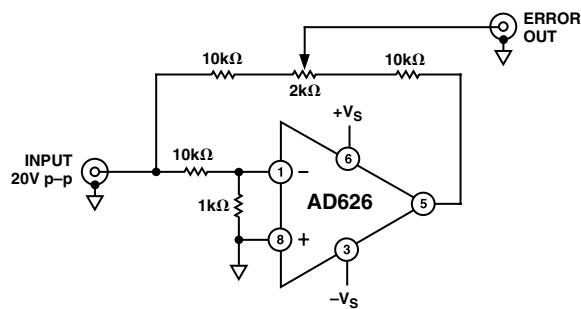
TPC 25. Settling Time. $V_S = +5 V$, $G = 10$ TPC 26. Settling Time. $V_S = +5 V$, $G = 100$ 

Figure 3. Settling Time Test Circuit

THEORY OF OPERATION

The AD626 is a differential amplifier consisting of a precision balanced attenuator, a very low drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages (V_{CM}), without the use of any other active components.

Figure 4 shows the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to dual resistive attenuators R1 through R4 whose purpose is to reduce the peak common-mode voltage at the input to the preamplifier—a feedback stage based on the very low drift op amp A1. This allows the differential input voltage to be accurately amplified in the presence of large common-mode voltages six times greater than that which can be tolerated by the actual input to A1. As a result, the input CMR extends to six times the quantity ($V_S - 1 V$). The overall common-mode error is minimized by precise laser-trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio (CMRR) of at least 10,000:1 (80 dB).

To minimize the effect of spurious RF signals at the inputs due to rectification at the input to A1, small filter capacitors C1 and C2 are included.

The output of A1 is connected to the input of A2 via a 100 kΩ (R12) resistor to facilitate the low-pass filtering of the signal of interest (see Low-Pass Filtering section).

The 200 kΩ input impedance of the AD626 requires that the source resistance driving this amplifier be low in value (<1 kΩ)—this is

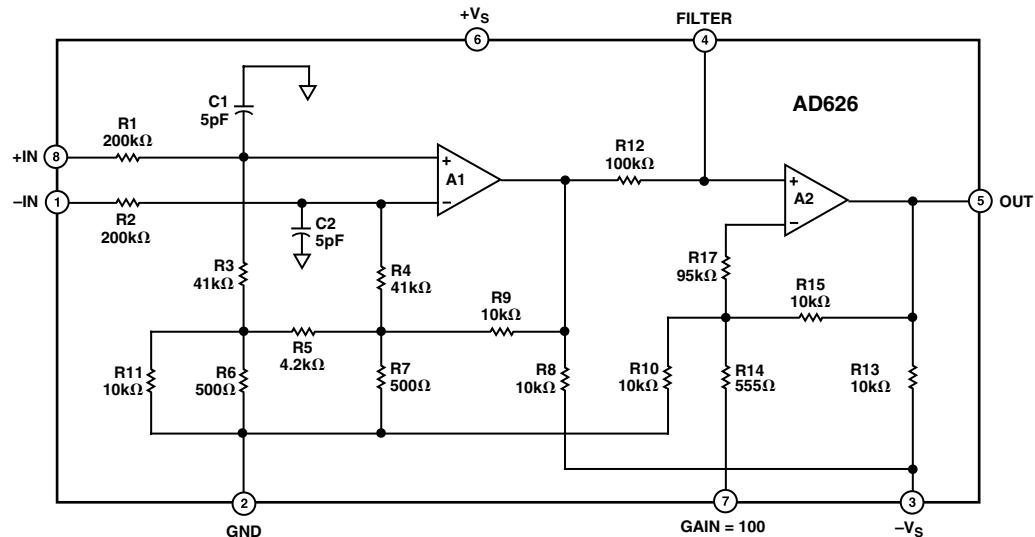


Figure 4. Simplified Schematic

AD626

necessary to minimize gain error. Also, any mismatch between the total source resistance at each input will affect gain accuracy and common-mode rejection (CMR). For example: when operating at a gain of 10, an $80\ \Omega$ mismatch in the source resistance between the inputs will degrade CMR to 68 dB.

The output buffer, A2, operates at a gain of 2 or 20, thus setting the overall, precalibrated gain of the AD626 (with no external components) at 10 or 100. The gain is set by the feedback network around amplifier A2.

The output of amplifier A2 relies on a $10\ \text{k}\Omega$ resistor to $-V_S$ for "pull-down." For single-supply operation, ($-V_S = \text{"GND"}$), A2 can drive a $10\ \text{k}\Omega$ ground referenced load to at least $+4.7\ \text{V}$. The minimum, nominally "zero," output voltage will be $30\ \text{mV}$. For dual-supply operation ($\pm 5\ \text{V}$), the positive output voltage swing will be the same as for a single supply. The negative swing will be to $-2.5\ \text{V}$, at $G = 100$, limited by the ratio:

$$-V_S \times \frac{R_{15} + R_{14}}{R_{13} + R_{14} + R_{15}}$$

The negative range can be extended to $-3.3\ \text{V}$ ($G = 100$) and $-4\ \text{V}$ ($G = 10$) by adding an external $10\ \text{k}\Omega$ pull-down from the output to $-V_S$. This will add $0.5\ \text{mA}$ to the AD626's quiescent current, bringing the total to $2\ \text{mA}$.

The AD626's 100 kHz bandwidth at $G = 10$ and 100 (a 10 MHz gain bandwidth) is much higher than can be obtained with low power op amps in discrete differential amplifier circuits. Furthermore, the AD626 is stable driving capacitive loads up to $50\ \text{pF}$ (G10) or $200\ \text{pF}$ (G100). Capacitive load drive can be increased to $200\ \text{pF}$ (G10) by connecting a $100\ \Omega$ resistor in series with the AD626's output and the load.

ADJUSTING THE GAIN OF THE AD626

The AD626 is easily configured for gains of 10 or 100. Figure 5 shows that for a gain of 10, Pin 7 is simply left unconnected; similarly, for a gain of 100, Pin 7 is grounded, as shown in Figure 6.

Gains between 10 and 100 are easily set by connecting a variable resistance between Pin 7 and Analog GND, as shown in Figure 7. Because the on-chip resistors have an absolute tolerance of $\pm 20\%$ (although they are ratio matched to within 0.1%), at least a 20% adjustment range must be provided. The values shown in the table in Figure 7 provide a good trade-off between gain set range and resolution, for gains from 11 to 90.

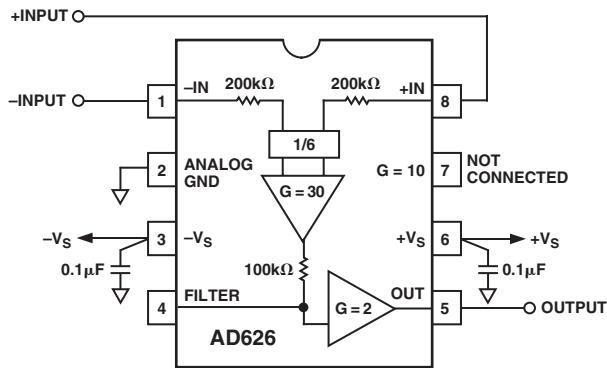


Figure 5. AD626 Configured for a Gain of 10

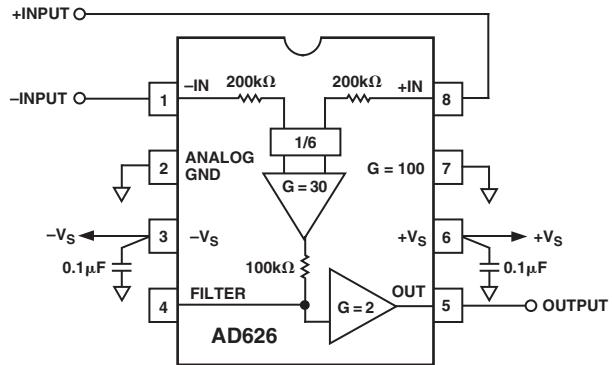
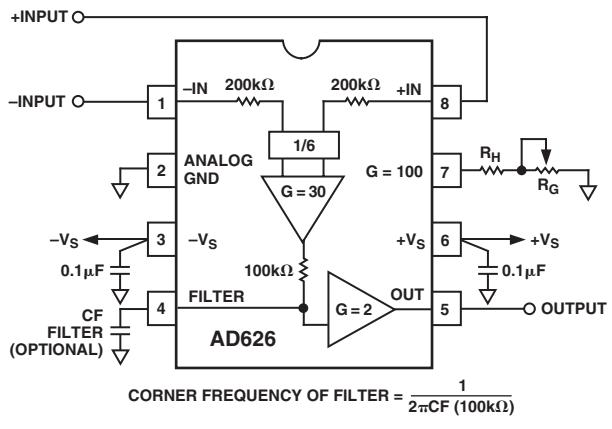


Figure 6. AD626 Configured for a Gain of 100



CORNER FREQUENCY OF FILTER = $\frac{1}{2\pi CF (100\text{k}\Omega)}$

RESISTOR VALUES FOR GAIN ADJUSTMENT

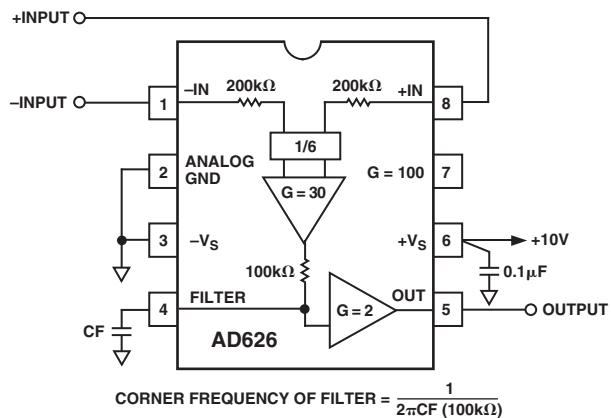
GAIN RANGE	$R_G(\Omega)$	$R_H(\Omega)$
11 - 20	100k	4.99k
20 - 40	10k	802
40 - 80	1k	80
80 - 100	100	2

Figure 7. Recommended Circuit for Gain Adjustment

SINGLE-POLE LOW-PASS FILTERING

A low-pass filter can be easily implemented by using the features provided by the AD626.

By simply connecting a capacitor between Pin 4 and ground, a single-pole low-pass filter is created, as shown in Figure 8.



CORNER FREQUENCY OF FILTER = $\frac{1}{2\pi CF (100\text{k}\Omega)}$

Figure 8. A One-Pole Low-Pass Filter Circuit Which Operates from a Single +10 V Supply

CURRENT SENSOR INTERFACE

A typical current sensing application, making use of the large common-mode range of the AD626, is shown in Figure 9. The current being measured is sensed across resistor R_S . The value of R_S should be less than $1\text{ k}\Omega$ and should be selected so that the average differential voltage across this resistor is typically 100 mV.

To produce a full-scale output of +4 V, a gain of 40 is used adjustable by $\pm 20\%$ to absorb the tolerance in the sense resistor. Note that there is sufficient headroom to allow at least a 10% overrange (to +4.4 V).

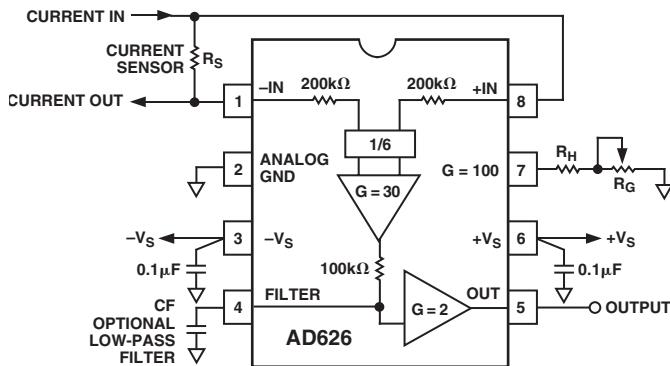


Figure 9. Current Sensor Interface

BRIDGE APPLICATION

Figure 10 shows the AD626 in a typical bridge application. Here, the AD626 is set to operate at a gain of 100, using dual-supply voltages and offering the option of low-pass filtering.

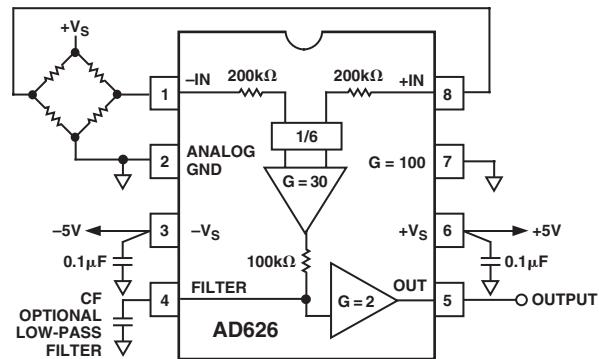
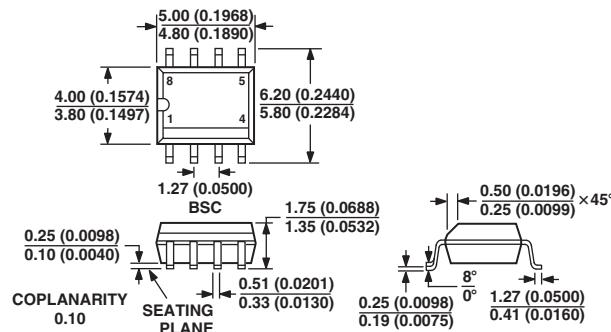


Figure 10. A Typical Bridge Application

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

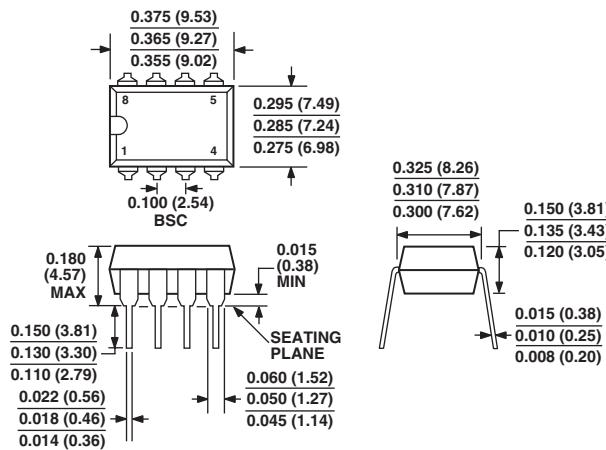
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual-In Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
1/03—Data Sheet changed from REV. C to REV. D.	
Renumbered Figures and TPCs	Universal
Edits to Figure 1	1
Edits to SPECIFICATIONS, Output	3
Edit to ORDERING GUIDE	4
Update to standard CAUTION/ESD Warning note and diagram	4
Edits to TPC 8	6
Updated OUTLINE DIMENSIONS	12